H E R M E S

Efficient Ring Packing using MLWE Ciphertexts and Application to Transciphering

Youngjin Bae, Jung Hee Cheon, Jaehyung Kim, <u>Jai Hyun Park</u>, Damien Stehlé

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• Ring packing (RP) bridges LWE and RLWE formats [CGGII7, MS18, BGGJ20, CDKS21, LHH+21]

Ring packing

- Scheme switching during homomorphic computation
- Transciphering

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- Parameters: Moduli and Ring degree
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	- Requires large evaluation keys.

Accelerating FHE RP

Conventional approach

Ring switching (RS) [GHPS13]

- Small moduli allow a small degree RLWE.
- Switch into RLWE of an extension ring with a higher degree.

Improved FHE RP

Existing Approaches
• LWE ciphertexts ct_i : $c_{i,1} s_1 + c_{i,2} s_2 + \cdots + c_{i,K} s_K \approx m_i$ for each *i*

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RP as a Matrix Multiplication

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• RP is (plaintext) matrix – (ciphertext) vector multiplication in RLWE formats.

Existing Approaches

• Three approaches to encode the plaintext matrix.

Column method

- CGGI17, BGGJ20
- \bullet K key switchings
- \bullet K keys
- Consumes 0 level

Row method

- CDKS21
- \bullet K key switchings
- \cdot log K keys
- Consumes 1 level

Diagonal method

- HS14, LHH+21
- $2\sqrt{K}$ key switchings
- $2\sqrt{K}$ keys
- Consumes ≥ 4 levels

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HERMES¹ : the *block method* with our optimizations

• How to encode the blocks?

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- How to squeeze the blocks? *MLWE key switching / MLWE ring switching*

Experimental Results

Ring Packing

All experiments are measured on AMD® Ryzen 7 3700x 8-core processor with a single-threaded CPU. Pegasus figures are borrowed from [LHH+21]; measured on single-threaded Intel Xeon Platinum 8269CY CPU (20-cores) at 2.50GHz.
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Transciphering

All experiments are measured on AMD® Ryzen 7 3700x 8-core processor with a single-threaded CPU. HERA and Rubato figures are borrowed from [CHK+21] and [HKL+22]; measured on AMD Ryzen 7 2700X @ 3.70 GHz single-threaded CPU.

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